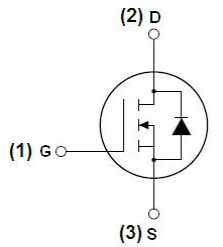
4N80

800V N-Plance Enhancement Mode MOSFET

Description

The 4N80 series are from the innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance



General Features

VDS =800V,ID =4A

RDS(ON) <2.5Ω@ VGS=10V

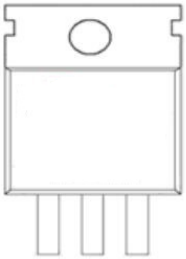
Application

100% UIS Test

Simple Drive Requirement

Fast Switching Characteristic

RoHS Compliant & Halogen-Free



Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Rating	Units
VDS	Drain-Source Voltage	800	V
VGS	Gate-Source Voltage	±30	V
I_D@T_C=25℃	Drain Current, V_{GS} @ 10V[3]	4	A
IDM	Pulsed Drain Current[1]	16	A
P_D@T_C=25℃	Total Power Dissipation	32.9	W
P_D@T_A=25℃	Total Power Dissipation	1.92	W
E_{AS}	Single Pulse Avalanche Energy[4]	8	mJ
TSTG	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃
Rthj-c	Maximum Thermal Resistance, Junction-case	3.8	℃/W
Rthj-a	Maximum Thermal Resistance, Junction-ambient	65	℃/W

800V N-Plance Enhancement Mode MOSFET

Absolute Maximum Ratings@T_j=25ºC(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	800	-	-	V
RDS(ON)	Static Drain-Source On-Resistance[2]	V_{GS}=10V, I_D=2A	-	-	2.5	Ω
VGS(th)	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	2.5	-	4.5	V
g_{fs}	Forward Transconductance	V_{DS}=20V, I_D=2A	-	5.3	-	S
IDSS	Drain-Source Leakage Current	V_{DS}=640V, V_{GS}=0V	-	-	100	uA
IGSS	Gate-Source Leakage	V_{GS}=±30V, V_{DS}=0V	-	-	±1	uA
Q_g	Total Gate Charge	I_D=4A V_{DS}=640V V_{GS}=10V	-	27	43.2	nC
Q_{gs}	Gate-Source Charge		-	4	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge		-	15	-	nC
td(on)	Turn-on Delay Time	V_{DD}=400V I_D=4A R_G=25Ω V_{GS}=10V	-	14	-	ns
t_r	Rise Time		-	30	-	ns
td(off)	Turn-off Delay Time		-	69	-	ns
t_f	Fall Time		-	34	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V V_{DS}=100V f=1.0MHz	-	680	1088	pF
Coss	Output Capacitance		-	40	-	pF
C_{rss}	Reverse Transfer Capacitance		-	10	-	pF
R_g	Gate Resistance	f=1.0MHz	-	3.7	7.4	Ω
VSD	Forward On Voltage[2]	I_S=4A, V_{GS}=0V	-	-	1.5	V
trr	Reverse Recovery Time	I_S=4A, V_{GS}=0V dI/dt=100A/μs	-	430	-	ns
Q_{rr}	Reverse Recovery Charge		-	1.9	-	uC

Notes:

1.Pulse width limited by max. junction temperature.

2.Pulse test

3.Ensure that the junction temperature does not exceed T_{Jmax}..

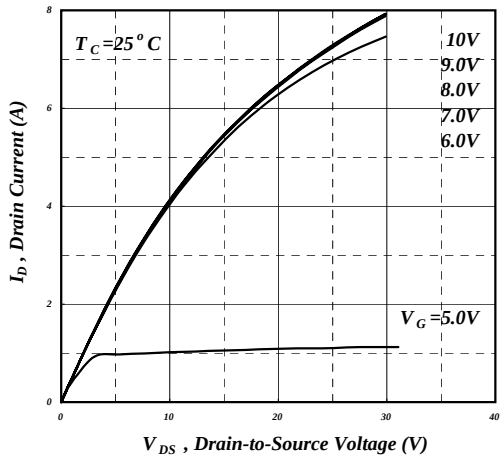


Fig 1. Typical Output Characteristics

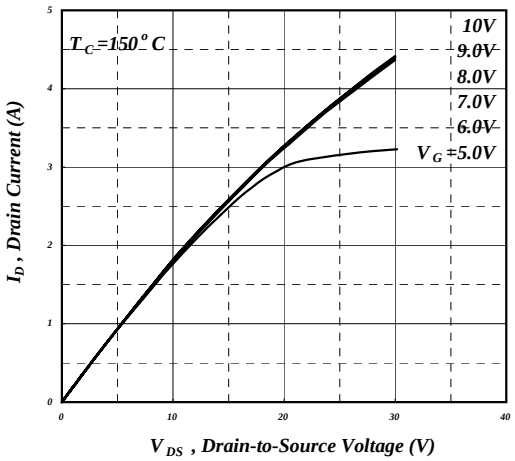


Fig 2. Typical Output Characteristics

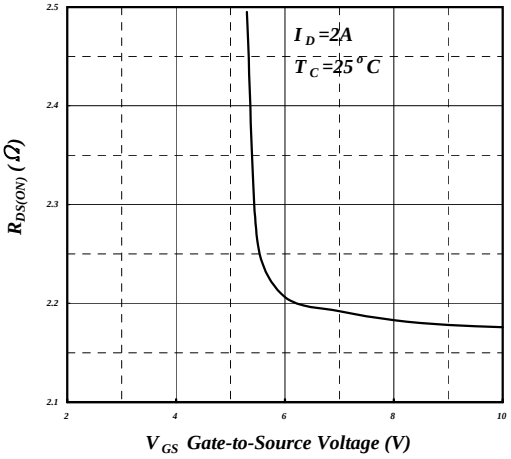


Fig 3. On-Resistance v.s. Gate Voltage

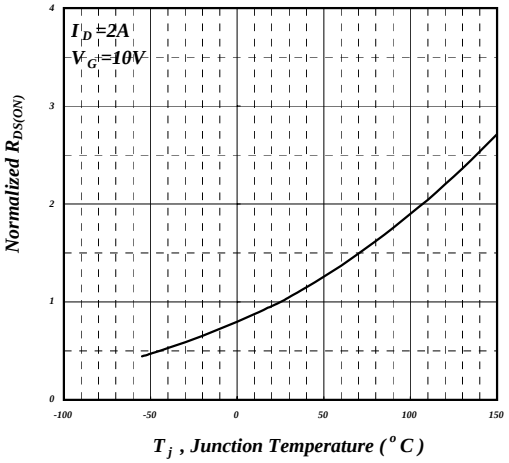


Fig 4. Normalized On-Resistance v.s. Junction Temperature

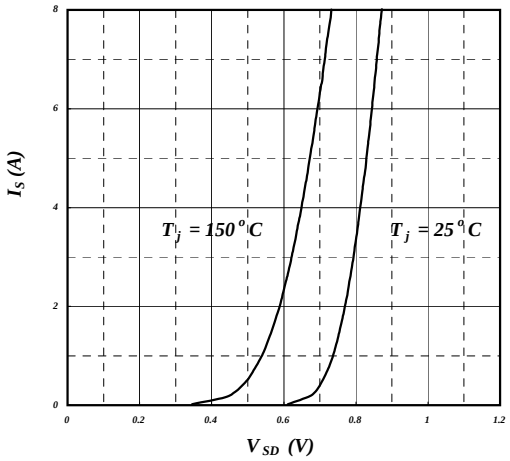


Fig 5. Forward Characteristic of Reverse Diode

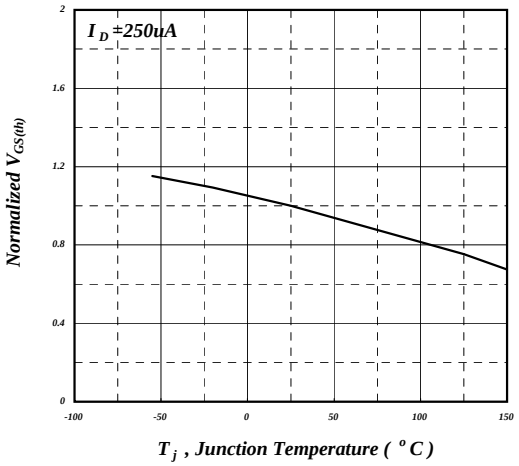


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

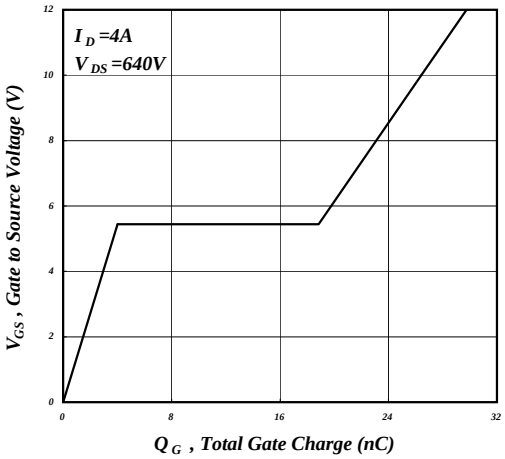


Fig 7. Gate Charge Characteristics

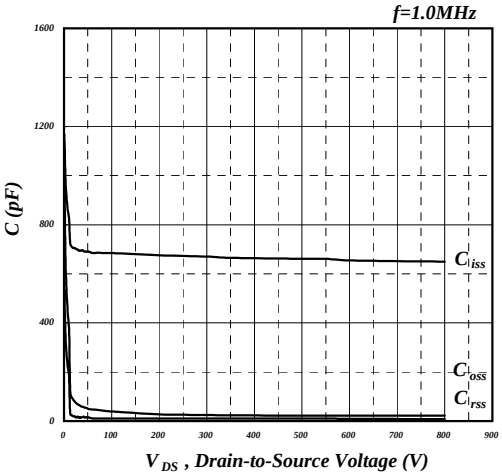


Fig 8. Typical Capacitance Characteristics

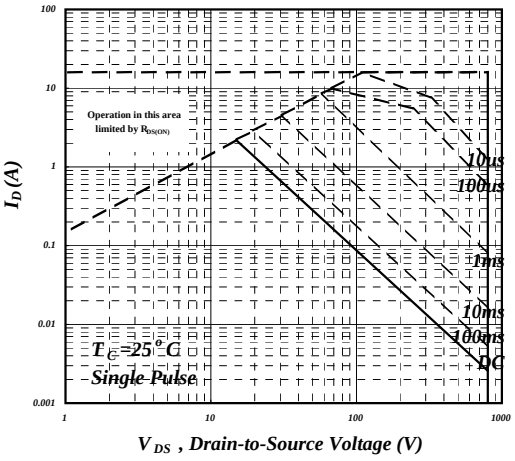


Fig 9. Maximum Safe Operating Area

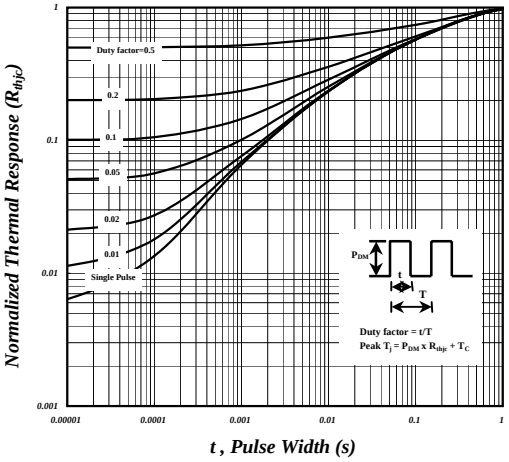


Fig10. Effective Transient Thermal Impedance

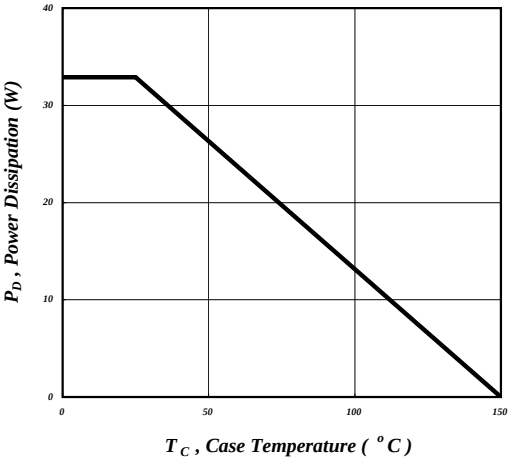


Fig 11. Total Power Dissipation

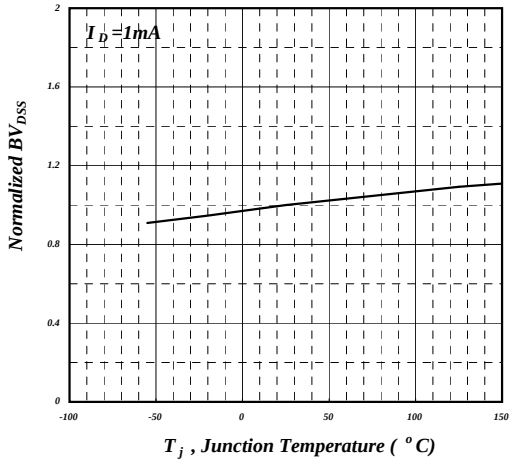
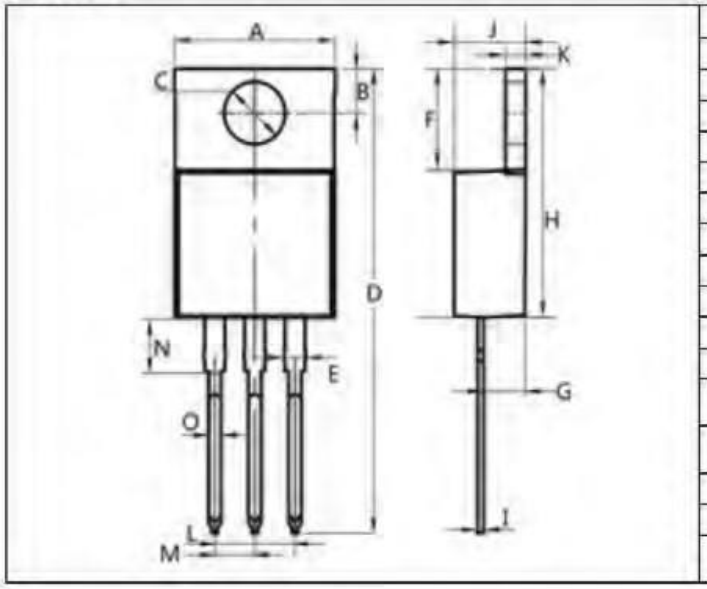


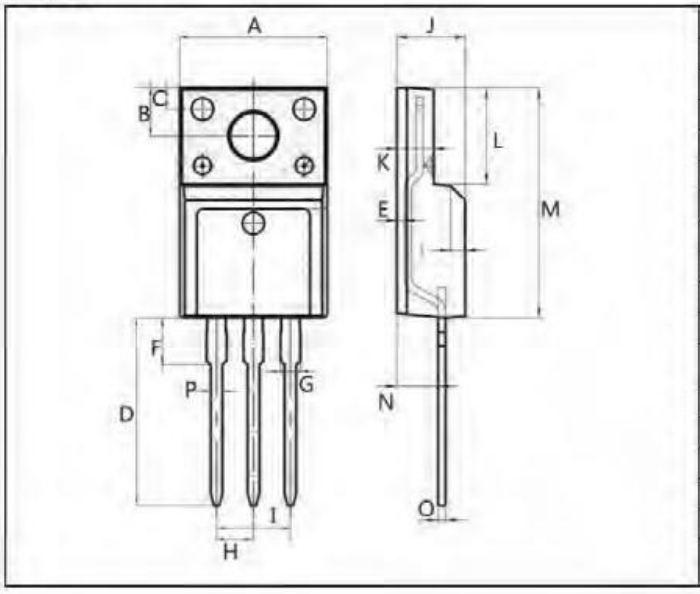
Fig 12. Normalized BV_{DSS} v.s. Junction Temperature

TO-220AB



Dim.	Min.	Max.
A	10.0	10.4
B	2.5	3.0
C	3.5	4.0
D	28.0	30.0
E	1.1	1.5
F	6.2	6.6
G	2.9	3.3
H	15.0	16.0
I	0.35	0.45
J	4.3	4.7
K	1.2	1.4
L	Typ 5.08	
M	Typ 2.54	
N	3.1	3.5
O	0.7	0.9
All Dimensions in millimeter		

TO-220F



Dim.	Min.	Max.
A	9.9	10.3
B	2.9	3.5
C	1.15	1.45
D	12.75	13.25
E	0.55	0.75
F	3.1	3.5
G	1.25	1.45
H	Typ 2.54	
I	Typ 5.08	
J	4.55	4.75
K	2.4	2. 7
L	6.35	6.75
M	15.0	16.0
N	2.75	3.15
O	0.45	0.60
P	0.7	0.9
All Dimensions in millimeter		